Volatile Memory Motifs:
Minimal Spiking Neural Networks

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How spiking neuronal networks encode memories in their different time and spatial scales constitute a fundamental topic in neuroscience and neuro-inspired engineering. Much attention has been paid to large networks and long-term memory, for example in models of associative memory. Smaller circuit motifs may play an important complementary role on shorter time scales, where broader network effects may be of less relevance. Yet, compact computational models of spiking neural networks that exhibit short-term volatile memory and actively hold information until their energy source is switched off, seem not fully understood. Here we propose that small spiking neural circuit motifs may act as volatile memory components. A minimal motif consists of only two interconnected neurons – one self-connected excitatory neuron and one inhibitory neuron – and realizes a single-bit volatile memory. An excitatory, delayed self-connection promotes a bistable circuit in which a self-sustained periodic orbit generating spike trains co-exists with the quiescent state of no neuron spiking. Transient external inputs may straightforwardly induce switching between those states. Moreover, the inhibitory neuron may act as an autonomous turn-off switch. It integrates incoming excitatory pulses until a threshold is reached after which the inhibitory neuron emits a spike that then inhibits further spikes in the excitatory neuron, terminating the memory. Our results show how external bits of information (excitatory signal), can be actively held in memory for a pre-defined amount of time. We show that such memory operations are robust against parameter variations and exemplify how sequences of multidimensional input signals may control the dynamics of a many-bits memory circuit in a desired way.

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I. INTRODUCTION

Memory plays a fundamental role in biological, bio-inspired and abstract artificial computing systems. While in standard computers memory is usually implemented as discrete components [1], which can be addressed by other components as needed, in self-organized dynamical systems, computation and memory are typically intertwined, with computation and memory access taking place concurrently [2, 3]. In particular, neural networks are composed of many discrete computing units called neurons with memory being stored in the network's connectivity itself. The result of a computation is the observable emergent collective dynamics.

Due to its parallel and distributed nature, memory studies on neural networks have traditionally focused on large-scale systems, which not only exhibit a variety of emerging phenomena but also may become analytically tractable in the limit of large networks ($N \to \infty$) [4]. One key example of such collective phenomena is associative memory, in which memories are represented as attractors in state space, such that partial initial information or corrupted input signals may be sufficient to recover original stored associated memories. Most neural networks models, for memory or computation, are also non-volatile [5, 6], such that the information stored in the connections need not to be actively maintained but stay long-term without ongoing energy inputs required. Volatility, however, may be essential for a variety of cognitive functions, as working memory and real-time planning [7, 8], in particular on shorter timescales, where broader network effects may be of a lesser relevance.

Here we propose spiking neural network motifs to act as volatile memory components. A minimal example is composed of only two interconnected neurons (see Figure 1), one excitatory neuron with a delayed self-connection (autapse) and one inhibitory neuron, yielding a bistable motif circuit. A self-sustained periodic spike-train, representing an 'on' state and thus a bit '1' co-exists with the quiescent state, representing an 'off'-state and thus a bit '0'. Switching between those states is controlled by transient external inputs to either the inhibitory or the excitatory neuron. Alternatively, the inhibitory neuron may also act as an autonomous off switch for the circuit. That neuron integrates the pulses incoming from the excitatory neuron until it reaches a spiking threshold upon which the inhibitory neuron emits a spike and terminates the self-sustained periodic spike-train at the excitatory neuron, overall turning the collective motif state from '1' to '0'. Collections of such motif may be used in parallel to represent more complex information as independent bits, if larger-scale network effects are not desirable or not relevant .

Our results below show how an external bit of information can be actively held in memory for a pre-defined amount of time. To hold a '1' bit in memory, neural spiking activity and thus energy is needed, making the memory system volatile. The small neural circuits
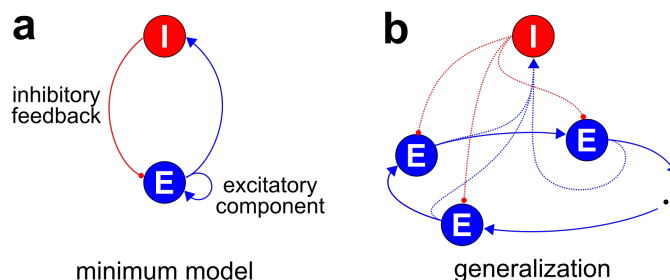

FIG. 1. **Spiking neural circuit motifs that implement a 1-bit volatile memory.** Blue circles labeled as 'E' represent excitatory neurons, red circles labeled as 'I' represent inhibitory neurons, circles as arrow heads represent inhibitory connections and conventional arrows represent excitatory connections. **(a)** A minimal circuit composed of two neurons, one excitatory and one inhibitory. **(b)** A circuit composed of an excitatory ring sub-network and an inhibitory neuron. **(a-b)** In both cases, the excitatory component has self-connections and connections to the inhibitory neurons while the inhibitory feedback connects to all excitatory neurons.

introduced below may serve as basic memory units for short-term volatile memory, and thus may complement the broad variety of previously proposed computational neural circuits and memory models [5, 9, 10], in particular the set of, also volatile, computing paradigms emerging in symmetrical systems [11–14] or stochastic dynamics in random networks with local excitation and global inhibition [15, 16], which also take advantage of self-organization instead of carefully tuned (many) connections between neurons.

II. MINIMAL MODEL OF NEURONAL NETWORK MOTIF

In this work we present a compact neuronal circuit motif that implements a 1-bit volatile memory. Volatile in this context means that spike activity, and thus energy, is needed to maintain at least one of the memory states. The system is compact because it can be implemented with as few as two neurons. For instance, as we sketch in Figure 1a, the system may be implemented with one inhibitory neuron and one excitatory neuron only. The connectivity is such that the excitatory neuron has a self connection and a connection to the inhibitory neuron; the inhibitory neuron has a single connection to the excitatory neuron. Alternatively, the excitatory component may be composed of a ring (Figure 1b) or other small population of neurons to better resemble a biological neural circuit or to otherwise circumvent self-connections. To explain the basic mechanisms and collective dynamics underlying volatile memory function of such motifs, we consider a minimal motif of two neurons in the remainder of this article.

For clarity of presentation we here mathematically describe the neurons as Leaky Integrate-and-Fire neuron models that exhibit parameters with a direct physical meaning also for potential hardware implementations. Leaky integrate-and-fire models already capture main fundamental features of spiking neurons, including their dynamics exhibiting two different times scales: a long term sub-threshold dynamics and short term interactions (spikes) modeled via discrete pulse responses. Our specific model is defined by a pair of differential equations,

$$\frac{dV_E}{dt} = A_E + \xi_E(t) - \gamma_E V_E + \sum_{t_i \in P_E} \varepsilon_E \delta(t - t_i - \tau_E) + \sum_{t_j \in P_I} \varepsilon_I \delta(t - t_j - \tau_I) + \eta_E(t) \ (1)$$

$$\frac{dV_I}{dt} = A_I + \xi_I(t) - \gamma_I V_I + \sum_{t_i \in P_E} \varepsilon_E \delta(t - t_i - \tau_E) + \eta_I(t) \tag{2}$$

complemented by conditions for spike emission and reset. Specifically, we say that neuron $X \in \{E, I\}$ emits a spike at time $t := t_n$ if its voltage reaches a threshold,

$$V_X(t) \geq \theta$$

after which that voltage is reset to

$$V(t^+) := 0.$$

The time t_n indicates the nth spike time in the motif circuit (after some reference time t_0). Moreover, the parameters A_X represent temporally the internal driving currents that set the equilibrium voltage (see below), $\xi_X(t)$ external driving currents serving as input signal to store or remove memories, and γ_X the leak constants. Finally ε_X represent the connection weights, τ_X the delays between a spike emitted by neuron X and reception of that spike and P_X denotes the set of all pulses elicited by a neuron X. The indices E and I indicate features of the excitatory and inhibitory neurons, respectively. Finally the inputs η_X are the contribution of internal noise. We remark that the autonomous part of the system of equations above, i.e. for $\eta_X(t) = \xi_X(t) \equiv 0$, has an analytical solution in between spike events and equally enable a piecewise, exact event-based simulations [17–19].

III.   SELF-SUSTAINED AND SELF-TERMINATED MEMORY

In the 2-unit motif network, two qualitatively different collective dynamics coexist (Figure 2), one exhibiting a self-sustained spike train created by the excitatory neuron, encoding a bit value '1', the other a quiescent state with no spikes emitted, encoding the bit value '0'. To store the value '1', an excitatory signal ξ_E is sent to the excitatory neuron; to switch from a bit '1' to zero, an external excitatory signal ξ_I is sent to the inhibitory neuron. Both types of external signals ξ_X need to be sufficiently strong, i.e. of sufficiently large amplitude and duration. The exact shape of these input signals as a function of time is not relevant as long as they are sufficiently rapid and charge the targeted neuron sufficiently for it to cross threshold and spike.

In the absence of external input signals, the voltage of both neurons with time tends towards their respective fixed points $V_E := I_E/\gamma_E$ and $V_I := A_I/\gamma_I$, see Figure 2 before input onset. A short transient input signal ξ_E triggers the release of the first spike by the excitatory neuron. In turn, this spike arrives in both neurons after a delay τ_E. For sufficiently strong pulse (response) amplitudes ε_E, the excitatory neuron sends a second spike and the process repeats. The motif network then maintains a spike-train with frequency $1/\tau_E$ until it is interrupted by an inhibitory pulse. There are two different mechanisms potentially causing such an interruption. First, a strong excitatory signal $\xi_I(t)$ could be sent at any desired time from outside the motif, see Figure 2a. Second, these systems hold the option of self-sustained and self-terminating memory function (see Figure 2b), with memory duration set by system parameters (that might, in turn, be varied on demand): The ongoing sequence of excitatory pulses fed into the inhibitory neuron promotes consecutive voltage jumps. If one such spike brings the inhibitory neuron to or beyond its firing threshold, the inhibitory neuron elicits a spike that after a delay τ_I causes a voltage leak in the excitatory neuron, thereby interrupting the self-sustained spike-train.
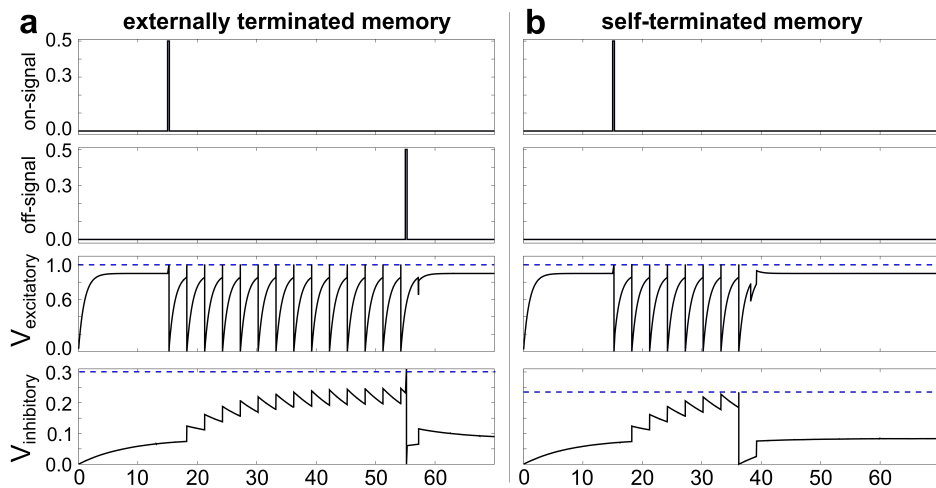

FIG. 2. **Bistable dynamics: memory initiation and termination.** For both panels, the upper graphs represent input currents as a function of time while the lower ones represent the voltages of inhibitory and excitatory neurons.**(a)** After a short input signal (upper panel), the excitatory neuron switches from its quiescent state to a self-sustained active state.A second external signal drives the inhibitory neuron to spike, which in turn terminates the memory, back to the quiescent state. **(b)** After the memory is initiated, the excitatory feedback loop persists until the inhibitory neuron produces a pulse, triggered by the consecutive excitatory pulses, thus terminating the memory. Parameters are: $A_E = 0.9$, $A_I = 0.01$, $\gamma_E = 1$, $\gamma_I = 0.12$, $\theta_E = 1$, $\theta_I = 0.3$, $\tau_E = 3$, $\tau_I = 2$, $\varepsilon_E = 0.05$, $\varepsilon_I = -0.2$.

IV. MEMORY DURATION

An interesting feature of the memory circuit motif presented is its tunable memory duration. Quantitatively, how long the an on-state is held active before self-terminating depends on most of the system parameters, for example on the pulse amplitudes (and durations), the delays, and the leak constant γ_X. For a qualitative analysis, we study the memory duration in terms of variations of the leakage parameter γ_I and the firing threshold θ_I, fixing all other parameters. A natural way to measure the memory duration is in terms of number of elicited spikes; the absolute real time again depends on chosen parameters set in any motif implementation. Furthermore, because the excitatory neuron's role is simply to generate a spike-train with a fixed frequency $1/\tau_E$, we here studied the memory duration from the perspective of the inhibitory neuron's response to such spike-trains.

As shown in Figure 3a, if γ_I is large enough, most of the current injected into a neuron is lost during the inter-spike intervals and the voltage curve resembles a non-linear saw wave with a small up-drift. Contrariwise, in the limit of $\gamma_I \to 0$, no current is lost, as there is no leak term, and the voltage curve thus has a stair shape. Intermediary values show an average logarithmic increase overlayed by the spikes. Notice the exact values of γ_I shown in Figure 3 are only illustrative, as the same qualitative effects can be achieve for fixed γ_I and varying, for example, τ_E instead. We also expect the system to show robustness to small variations of ε_E as the leakage grows exponentially with the deviation from the resting state, see Figure 3b.

The memory duration is controllable. For depiction, we varied the firing threshold θ_I and fixed all other parameters. Figure 3c shows how larger γ_I values restrict the discernible memories' duration to a predefined interval of pulses, as the voltage peaks immediately after
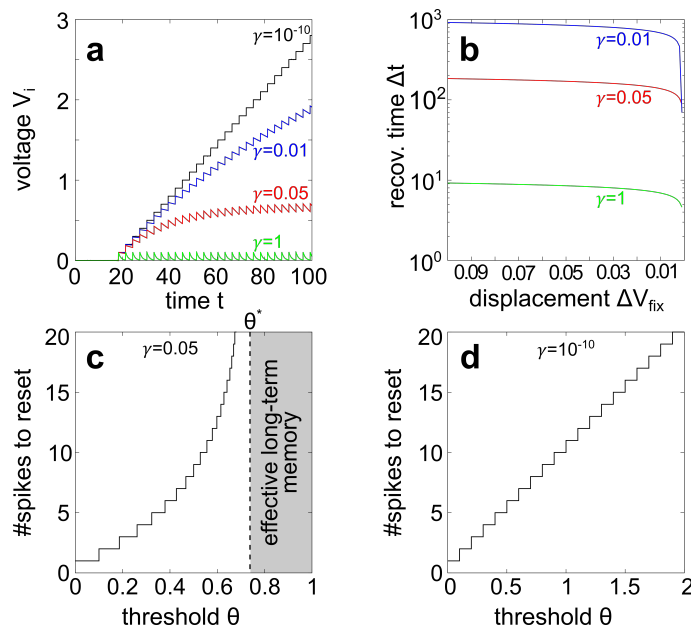

FIG. 3. **Memory duration and long-term dynamics (a)** Dynamical response of the inhibitory neuron to long spike trains with fixed frequency and amplitude. The larger the leak constant γ_I, the slower the voltage increases on average. **(b)** Given an instantaneous voltage jump ΔV_{fix} at time t_0 from the resting state, this panel shows the recovery time Δt, in which the voltage is $V(\Delta t) - V_I = 10^{-5}$ away from its resting states. The larger the leak constant γ_I, the shorter the recovery time for the same ΔV_{fix}. **(c)** Number of spikes received by the inhibitory neuron until reset as a function of its threshold θ. **(d)** As in **(c)**, but for a smaller $\gamma = 10^{-10}$. The smaller γ_I, the longer the curve resembles an equally spaced stair. Parameters: the same as in Figure 2 if not stated otherwise. $A_I = 10^{-4}$ for all panels.

consecutive spikes get closer exponentially fast. For large enough θ_I the memory duration is in practice long-term, as the actual difference between the voltage peaks (at spike times) decreases exponentially with θ_I and the voltage does not converge to the threshold in finite time or converge to a value below the threshold. For $\gamma_I \to 0$, the leak is negligible, and the memory duration increases in equally spaced steps, multiples of to the spike amplitude ε_E (Figure 3d). We remark that long-term memory in this context does not imply storage but long-lasting, as the memory here is always sustained by pulses and is, thus, still volatile.

V. INFLUENCE OF NOISE

Noise is an ever-present feature in biological and artificial (hardware) neural networks. Its role in memory and computation is varied and is often beneficial, in contrast to their effects in signal transmission lines. We now describe the effects of noise on our compact memory circuit. In the following, we add independent Gaussian noise sources $\eta_X(t)$, with identically distributed random components, to both neurons. The noise is modeled (approximated) by adding the term

$$\eta_X(t + \delta t) - \eta_X(t) = \sqrt{\delta t} N_{rand}(\sigma, 0) \tag{3}$$

to the righthand side of equations (1) and (2). Here $N_{rand}(\sigma, 0)$ is a random number drawn from a Gaussian distribution with variance σ and centered at zero. To conserve the event-based feature time evolution noise is evaluated after discrete times intervals δt drawn independently from a Poisson distribution with average $\langle \delta t \rangle = \tau_E/100$. That is, the noise sample intervals are randomized and independent for each neuron, while their average sampling interval is fixed.

Figure 4 illustrates the effect of different noise amplitudes for small and for intermediate
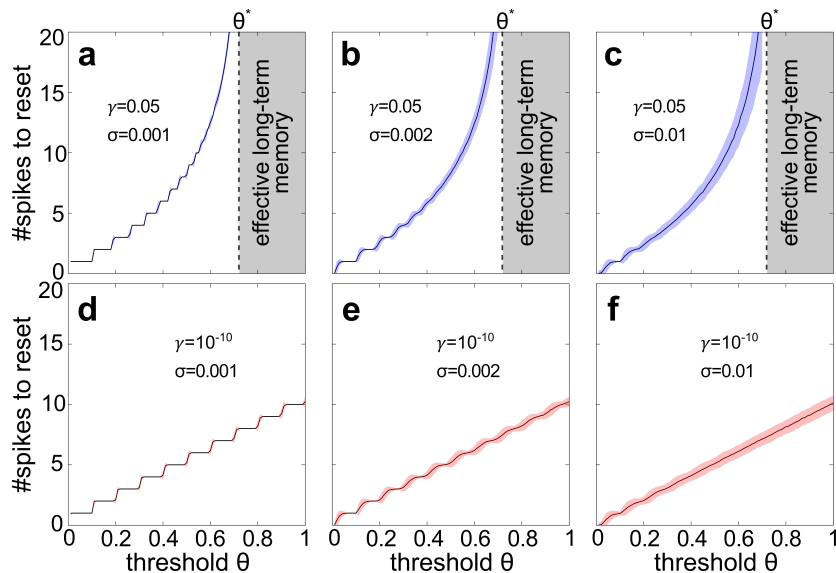

FIG. 4. **Noise-induced variability of memory duration.** Average number of spikes (black curves) received by the inhibitory neuron until its first spike and standard deviation (blue and red backgrounds) as functions of the inhibitory neuron's firing threshold. Measures calculated over 1000 repetitions at intervals of 0.01 volts. **(a-c)** For fixed γ_I, changing the noise standard deviation σ softens the staircase features of the curve. Even though the mean does not seem to deviate too far from the noiseless case, the standard deviation monotonically increases with θ. **(d-e)** Same results as in **(a-c)**, but with a slower increase rate. Parameters: same parameters as in Figure 3 if not stated otherwise.

noise amplitudes, $\gamma_I = 0.05$ and $\gamma_I = 10^{-10}$, respectively. Qualitatively, the results are the same in their most important aspects. Initially, for small σ, noise mostly affects the vicinity of the transition points between two memories duration (step jumps). As a result, the steps themselves become less steep than without noise. For larger noise strength σ, the plateaus (progressively) lose their identity, due to the large variability in the memory duration between random realizations, as also reflected in an increase in the standard deviation of the number of spikes to reset. Because the voltage plateaus for large γ_I become progressively smaller without noise, the increase in standard deviation becomes also progressively larger and more apparent with larger θ_I, compare Figure 4b-c to Figure 4e-f. Furthermore, combinations of small enough θ_I with large enough σ may promote eventual noise-induced spikes in the inhibitory neuron (false positive), even without an external signal to any of the neurons. As a consequence, spike events occur even before the excitatory neuron has its first spike, which translate in average memory duration below 1 in Figures 4(b-c) and Figures 4(e-f). Notice, 1 is the minimum memory length for the noise-free dynamics, that is, a single excitatory spike promoting an inhibitory spike.

VI. LOADING AND FLUSHING MULTI-DIMENSIONAL MEMORIES

In neuronal systems, sets of neurons or neuronal networks can be used to represent and store information. In our approach to transiently holding bits in memory, neurons are interconnected forming small motifs. In the simplest setting, multi-dimensional memories may thus be established by multiple motifs acting independently and in parallel. In such settings, multi-dimensional inputs can be loaded concurrently into memory as independent bits, not unlike in a traditional computer (see Figure 5). In our model, loading a bit in memory is intuitive and in line with traditional computer, each single bit can be set to one of two states almost instantaneously (within one spike cycle interval), independently of the current states of the neuron. Furthermore, this system exhibits a natural ground state (non-active), to which the system abruptly switch after the memory interval elapses. Moreover, the state representation is very convenient for binary codes, as one state has spike activity and the other has a complete absence of spikes, thus, it does not require involved decoding approaches.

Figure 5 shows how a sequence of words can be loaded into an array of neurons. As expected from our previous discussion around Figure 2, a new value can be loaded independent of the system state. The single false positive spikes after each active-to-quiescent change of states occurs due to the delay τ_I, i.e. spike signals still in transit (sent but not yet received). As a consequence, the desired system state, i.e. the collective
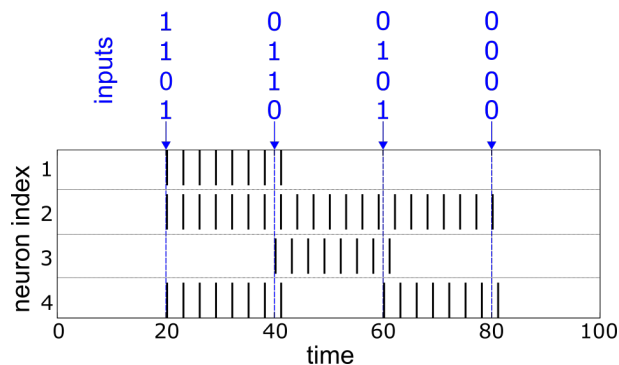

FIG. 5. **A sequence of four-bits words.** Only excitatory spikes are depicted. Four independent 1-bit neural circuit receive a sequence of four four-bits words. The last signal also serves to reset the system. Inputs label as 0 represent short inputs to the inhibitory neuron and as 1 to the excitatory neuron. In both cases the signal's duration is 0.3 and the amplitude is 0.5, see Figure 2 for details.

dynamics at all motifs, is assumed after a (small) lag time $\Delta t > \tau_I$. The exact timing depends on the excitatory neuron's voltage at the time it receives the inhibition. This observation sets a minimum of two consecutive pulses with frequency $1/\tau_E$ to guarantee a correct solution, because after a change in input signals, a single pulse may still be triggered by the former input signal (a false '1'). The real-world (clock) time interval τ_E, e.g. in seconds, is defined by the neuron model time scales, by choosing the units for τ_E.

VII.   DISCUSSION

We have proposed a general concept of implementing tunable volatile memory in simple neural networks. Such networks are small network motifs and exploit bi- or multistability to realize memory dynamically. Memory duration is either determined by system parameters that set the time scale of self-terminating a memory, or by external signals.

The concept of volatile memory is already familiar in computer science, see [20]. It is defined as a memory type that is actively maintained by the system, thus continuously consuming power. Contrary to storage, such memory is erased each time power is no longer provided to the system. Inspired by such concepts, we here proposed that simple neural motifs may act as volatile memory components. Our model is fundamentally different from previous neuronal models with similar functionality, which rely on, e.g., short-term plasticity ([21]), because our model requires no changes in the network connectivity or their weights. Instead, memory is held dynamically in the spike configuration until terminated internally or externally. We specifically analyzed a simple 1-bit volatile memory neural network motif that exhibit bi-stability. The bit '1' is represented by a self-sustained spike train and the bit '0' by no spiking activity.

Our focus on minimal motifs was motivated by two aspects: first, independent bits may play an important role in small systems, where network effects may be less relevant; second, the minimal 2-neuron systems offers maximal clarity in gaining insights about fundamental mechanisms that underlie both the self-organized collective dynamics of a motif and its response to external control signals. We remark that the same concept and mechanisms underlie also volatile memory dynamics in larger recurrent motifs that exhibit a suitable inhibitory component (shutdown-counter) and may thus self-terminate memory. In general, for larger motifs or several motifs embedded into a larger network, future work will need to investigate two aspects, local memory function and broader network effects. Larger motifs or networks may also hold the option for additional, potentially more advanced, functionality, for instance into the direction of systematically correlated multi-bit parallel memory storage, see also [13, 22].

We chose a standard leaky integrate-and-fire neuronal model [23–25] to keep the number of defining parameters to the most essential ones. Nevertheless, the conditions to implement such volatile memory circuit do not depend on the details of the neuronal model, but only on whether a self-sustained spike-train can be initiated by an external signal and whether the inhibitory feedback can promptly terminate such a spike-train. The results might thus be viewed as conceptual and largely independent of the neuron model.

Departing in some measure from the biological paradigm, independent bits (motif states) can be assembled to form larger sets of N motifs which combined have a large memory capacity (2^N), as in traditional computers. While it is unclear if the animal brain may take advantage of such combinatorial approach, bio-inspired computers can certainly make use of it to complement functionality of a large class of spiking neural systems, thereby maintaining information and processing completely within the spiking paradigm if desired.

Our minimal motif for volatile memory complements a variety of alternative dynamical system models of neural and networked information processing systems [26–29]. In particular, our model for short-term memory is a promising complement for approaches to computations relying on simple (neural) logical gates or on symmetrical spiking neural systems [11–14]. To date, these systems transiently process information but cannot retain the result of a computation, neither in the long- nor in the short-term, for example in (noisy) heteroclinic networks [12] or, more generally, networks of unstable states [13]. Finally, we believe that

such alternative and compact form of volatile memory implementation may contribute to future computing architectures, e.g., in neuromorphic and bio-inspired chemical, physical and robotic systems [30–33].

ACKNOWLEDGEMENTS

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